CLAIMS

What we claim is:

1. A method of analyzing power distribution in an integrated circuit chip comprising:

dividing a clock cycle of said integrated circuit chip into a plurality of time periods;

dividing said integrated circuit chip into a plurality of cells;

performing a static timing analysis for said plurality of cells to obtain current waveform data for each cell and each time period;

performing a power distribution analysis using said current waveform data.

2. The method according to claim 1, further comprising:

generating a pre-characterized cell library containing cell characterization data and using said cell characterization data to perform said static timing analysis.

3. The method according to claim 2, wherein said cell characterization data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

4. The method according to claim 1, further comprising:

physically designing said integrated circuit chip using said pre-characterized cell library.

5. The method according to claim 1, further comprising:

extracting parasitic resistors, capacitors and inductors to generate extracted signal net information which is used to perform said static timing analysis.

6. The method according to claim 4, wherein said current waveform data generated by an execution of said method is used to physically design said integrated circuit chip in a next execution of said method.

7. The method according to claim 1, wherein said static timing analysis determines when a current is required on said integrated circuit chip, an amount of current required on said integrated circuit chip, and where current is required on said integrated circuit chip.

8. The method according to claim 1, wherein every circuit on said integrated circuit chip switches within a given clock cycle.

9. The method according to claim 1, wherein said static timing analysis comprises:

disregarding circuits which cannot switch during a same time period.

10. The method according to claim 1, wherein each of said time periods is greater than or equal to a rise or fall time that captures 95% of signals on said integrated circuit chip.

11. The method according to claim 1, wherein said static timing analysis comprises:

assigning a charge used by a circuit to at least one time period; and

calculating node voltages for each time period.

12. The method according to claim 11, wherein said static timing analysis further comprises:

checking calculated node voltages against allowable limits;

calculating current densities using said calculated node voltages; and

checking said calculated node voltages against electromigration and local heating rules.

13. The method according to claim 11, wherein node voltages calculated during a run of said static timing analysis are back annotated in a next run of said static timing analysis to re-calculate node voltages.

14. The method according to claim 1, wherein said performing a power distribution analysis comprises generating a graphical map of a power distribution.

15. A system for analyzing power distribution in an integrated circuit chip comprising:

a chip design device for using pre-characterized cell data to logically and physically design said integrated circuit chip;

a power grid extracting device, for inputting physical design data from said chip design device and generating extracted signal net information; and

a static timing analysis tool, for inputting said extracted signal net information and said physical design data and generating current waveform data.

16. The system according to claim 15, further comprising:

a power distribution analysis tool, for inputting said current waveform data and generating power distribution data.

17. The method of according to claim 6, wherein said method is performed by using a digital data processing apparatus.

18. A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of analyzing power distribution in an integrated circuit chip, said method comprising:

dividing a clock cycle of said integrated circuit chip into a plurality of time periods;

dividing said integrated circuit chip into a plurality of cells;

performing a static timing analysis for said plurality of cells to obtain current waveform data for each cell and each time period;

performing a power distribution analysis using said current waveform data.

19. The system according to claim 15, wherein said pre-characterized cell data is contained within a pre-characterized cell library.

20. The system according to claim 15, wherein said pre-characterized cell data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

21. The system according to claim 15, wherein said power grid extracting device extracts parasitic resistors, capacitors and inductors from a physical design of said integrated circuit chip to generate extracted signal net information.

22. The system according to claim 15, wherein said current waveform data generated during an operation of said system is input to said chip design device during a next operation of said system to refine a physical design of said integrated circuit chip.

23. The system according to claim 15, wherein said static timing analysis tool determines when a current is required on said integrated circuit chip, an amount of current required on said integrated circuit chip, and where current is required on said integrated circuit chip.

24. The system according to claim 15, wherein every circuit on said integrated circuit chip switches within a given clock cycle.

25. The system according to claim 15, wherein said static timing analysis tool disregards circuits which cannot switch during a same time period.

26. The system according to claim 15, wherein said static timing analysis tool divides a clock cycle of said integrated circuit chip into a plurality of time periods, and wherein each of said time periods is greater than or equal to a rise or fall time that captures 95% of signals on said integrated circuit chip.

27. The system according to claim 15, wherein said static timing analysis tool assigns a charge used by a circuit to at least one time period, and calculates node voltages for each time period.

28. The system according to claim 27, wherein said static timing analysis tool checks calculated node voltages against allowable limits, electromigration rules and local heating rules, and calculates current densities using said calculated node voltages.

29. The system according to claim 28, wherein node voltages calculated during a static timing analysis are back annotated into said static timing analysis tool during a next static timing analysis to re-calculate node voltages.

30. The system according to claim 16, wherein said power distribution analysis tool generates a graphical map of a power distribution on said integrated circuit chip.

31. The programmable storage medium according to claim 18, wherein said method further comprises:

generating a pre-characterized cell library containing cell characterization data and using said cell characterization data to perform said static timing analysis.

32. The programmable storage medium according to claim 31, wherein said cell characterization data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

33. The programmable storage medium according to claim 31, wherein said method further comprises:

physically designing said integrated circuit chip using said pre-characterized cell library.

34. The programmable storage medium according to claim 18, wherein said method further comprises:

extracting parasitic resistors, capacitors and inductors to generate extracted signal net information which is used to perform said static timing analysis.

35. The programmable storage medium according to claim 33, wherein said current waveform data generated by an execution of said method is used to physically design said integrated circuit chip in a next execution of said method.

36. The programmable storage medium according to claim 18, wherein said static timing analysis comprises:

disregarding circuits which cannot switch during a same time period.

37. The programmable storage medium according to claim 18, wherein said static timing analysis comprises:

assigning a charge used by a circuit to at least one time period; and

calculating node voltages for each time period.

38. The programmable storage medium according to claim 18, wherein said static timing analysis further comprises:

checking calculated node voltages against allowable limits;

calculating current densities using said calculated node voltages; and

checking said calculated node voltages against electromigration and local heating rules.

39. The programmable storage medium according to claim 38, wherein node voltages calculated during a run of said static timing analysis are back annotated in a next run of said static timing analysis to re-calculate node voltages.

40. The programmable storage medium according to claim 18, wherein said performing a power distribution analysis comprises generating a graphical map of a power distribution on said integrated circuit chip.